way of a substitute specification, which includes no new matter. Claims 1 - 3, 7, 9, 11, 13 - 15, 17, and 19 have been amended. New claim 23 has been added. It is noted with appreciation that claims 15-22 are stated to be allowable. Since claims 15-22 also have been rejected under 35 USC 112, second paragraph, it is assumed that the Examiner merely intended to indicate that the claims 15-22 are allowable over the prior art. Reexamination and reconsideration of the amended application respectfully is requested.

The Examiner rejected claims 1-22 under 35 USC 112, second paragraph, as being indefinite, for reasons given with respect to claims 1, 7 and 11, namely that there is no antecedent basis for "the circuit board." The rejection is traversed because anticedent basis may be found in line 2 of each of claims 1, 7 and 11. Moreover, claims 1, 7 and 11 have been amended to more clear describe the relationship between the circuit board and the apparatus of the invention. Also, all of the amended claims include editorial amendments intended only for improved clarity without changing the scope. The rejection accordingly should be withdrawn.

The Examiner rejected claims 1-12 and 14-22 under 35 USC 103(a) as being unpatentable over *Yasunaga et al.* (hereinafter referred to as *Yasunaga*). Claims 1 - 3, 7, 9, 11, 14, 15, and 19 have been amended. It is submitted that the rejection is inapplicable to the amended claim 1 and its dependent claims 2 - 6, and the rejection of claims 7-12 and 14-22 is respectfully traversed.

Claim 1, as amended, is directed to a semiconductor apparatus, which includes a semiconductor device, a plurality of conductive posts electrically connected to the

semiconductor device, and means for mounting the device onto a circuit board by soldering, including a plurality of conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board, wherein a peripheral edge of a resin covering for sealing a surface of the semiconductor device and an outer edge of the conductive post are separated by a distance narrower than a height of the conductive post.

Thus, according to a feature of the invention described in Claim 1, a distance ("d" in Figs. 3-8) between a peripheral edge of a molding resin and an upper edge of a conductive post is narrower or smaller than a height of the conductive post. Therefore, the connecting or bonding conditions of the bumps can be recognized visually during a mounting process. Further, the bumps are arranged adjacent the peripheral edge of the molding resin. This serves to improve an ability of the apparatus to radiate away heat.

Such a semiconductor apparatus is neither shown nor suggested by *Yasunaga*. See, for example, Fig. 81 of *Yasunaga*, which clearly shows the distance between the peripheral side surface of the molding resin 1 to be greater, in fact multiple times greater, than the height of the conductive post 9. Therefore, the *Yasunaga* apparatus cannot provide the above described advantages of the invention that the connecting or bonding conditions of the bumps can be recognized visually during a mounting process and so substantially improve an ability of the apparatus to radiate heat away.

Claim 1 and claims 2-6 depending therefrom therefore are deemed to be clearly patentable over *Yasunaga*. The rejection of these claims accordingly should be withdrawn.

Claim 7 is directed to a semiconductor apparatus, which includes a semiconductor device, a plurality of conductive posts electrically connected to the semiconductor device, means for mounting the device onto a circuit board by soldering, including a plurality of conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board, and a molding resin covering a surface of the semiconductor device, wherein the molding resin is shaped to have a step along the entirety of a peripheral edge of the semiconductor device, the step having upper and lower level portions. As a result, connecting or bonding conditions of bumps can be visually recognized in a mounting process. Further, a bonding area between a conductive post and a bump is increased, so that reliability of such bonding is increased.

Such a semiconductor apparatus is neither shown nor suggested by *Yasunaga*. For example, see again Fig. 81 of *Yasunaga*, which clearly shows no evidence of a step along the entirety of a peripheral edge of the semiconductor device, the step having upper and lower level portions. Therefore, the *Yasunaga* apparatus cannot provide the above-described advantages of the invention that the connecting or bonding conditions of the bumps can be recognized visually during a mounting process.

Claim 7 and claims 8-10 depending therefrom therefore are deemed to be clearly patentable over *Yasunaga*. The rejection of these claims accordingly should be withdrawn.

Claim 11 is directed to the embodiment of the invention shown in Figs. 13-20. In this embodiment and according to claim 11, a semiconductor apparatus includes a semiconductor device, a plurality of conductive posts electrically connected to the semiconductor device, and means for mounting the device onto a circuit board by soldering, including a plurality of first conductive bumps respectively positioned on an outer end of each of the conductive posts for soldering onto the circuit board. A molding resin covers a surface of the semiconductor device without covering a peripheral side surface of each conductive post. An insulating layer is formed on a peripheral surface of the semiconductor device and between an upper surface of the semiconductor device and the conductive posts. The molding resin is shaped to have a peripheral side surface on the identical plane with the peripheral side surface of the semiconductor device.

Thus, according to this aspect of the invention, a peripheral side surface of a conductive post is not covered with a molding resin, so that connecting or bonding condition of bumps can be visually recognized in a mounting process. Further, the semiconductor device, including on a peripheral surface of the semiconductor device and between an upper surface of the semiconductor device and the conductive posts, is covered with an insulating layer, so that the semiconductor device is prevented from being electrically connected with the bumps, even if a bump melts

and extends over a side surface of the conductive post to the semiconductor device. The insulating layer may fill a groove formed in peripheral areas of the semiconductor device.

Such a semiconductor apparatus as defined in claim 11 is neither shown nor suggested by *Yasunaga*. For example, see again Fig. 81 of *Yasunaga*, which clearly shows a semiconductor device being covered with a molding resin, but illustrates none of the other features of the present invention described in the paragraph above. For example, the insulating layer 13 of *Yasunaga* referenced by the Examiner and shown in Fig. 3 surrounding the base of the post 9, is nowhere disclosed to be formed on a peripheral surface of a semiconductor device or between an upper surface of the semiconductor device and the conductive posts. Nor is a peripheral side surface of the conductive post 9 shown not to be covered with the molding resin 1.

Claim 11 and claims 12 and 14 depending therefore are deemed clearly to be patentable over *Yasunaga*. The rejection of these claims accordingly should be withdrawn.

The Examiner also rejected claim 13 under 35 USC 103(a) as being unpatentable over *Yasunaga* in view of *Taguchi*. The rejection respectfully is traversed.

Claim 13 depends from claim 11 and *Taguchi* fails to teach the features of the invention of claim 11 described above and missing from *Yasunaga*. Claim 13 therefore is patentable for at least the reasons advanced as to the patentability of

claim 11. Moreover, the applicant would note that according to *Taguchi*, a semiconductor device is not resin-molded. *Taguchi* illustrates in Figs. 1 and 13, a semiconductor device 12 having a step portion and bumps 22 and 23 formed to extend onto the step portion through an insulating layer 16. However, the insulating layer is not arranged in a groove formed at peripheral portion of the semiconductor device. Moreover, the bumps 22 and 23 extend into the groove. For that reason the teachings of *Taguchi*, make it difficult to prevent a short circuit generated between a bump and a semiconductor device. For these reasons, claim 13 is deemed clearly to be patentable over *Yasunaga* in view of *Taguchi*. The rejection accordingly should be withdrawn.

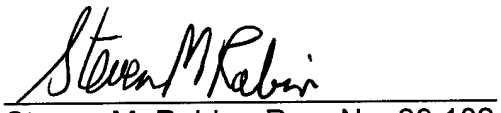
A new claim 23, depending from claim 11, has been added to further protect the invention. Submitted is a check in the amount of $18 in payment for this one new (excess) claim. If the check is missing or in an insufficient or excess amount, please charge of credit the overpayment of underpaying to our account number 18-0002, and advise us accordingly.

Based on the above, it is submitted that the application is in condition for allowance, and such a Notice, with allowed claims 1-23 is earnestly solicited.

Should the Examiner feel that a further conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the

undersigned counsel to arrange for such an interview.

Respectfully submitted,



October 3, 2002
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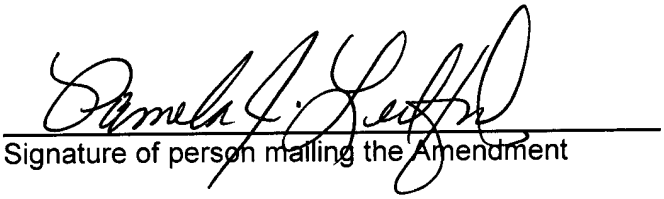
Certification Under 37 C.F.R. §1.8 (if applicable)

I hereby certify that this Amendment is being deposited with the United States Postal Service as First Class Mail under 37 C.F.R. §1.8 on this **October 3, 2002** and addressed to the Commissioner for Patents, Washington, D.C. 20231.

Pamela J. Ledford
Typed or printed name of person mailing the Amendment



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